CLAIMS

What is claimed is:

1. A mating detection circuit constructed and arranged to determine whether at least one connector of an expansion card is mated with a corresponding connector of a computer system in which the expansion card is configured to be installed.

2. The circuit of claim 1, wherein the mating detection circuit is further constructed and arranged to monitor at least one signal related to an associated signal presented at each of the at least one connector.

3. The circuit of claim 2, wherein for each of the at least one connector, each monitored signal is one of either the same as, provided by, derived from or controlled by the associated signal presented at the connector.

4. The circuit of claim 1, wherein the mating detection circuit generates at least one mating status signal each representing the mating status of a combination of one or more of the at least one connector.

5. The circuit of claim 4, wherein the at least one mating status signal is provided to the computer system.

6. The circuit of claim 5, wherein the at least one mating status signal controls a state of one or more bits in the computer system.

7. The circuit of claim 6, wherein the at least one mating status signal controls a state of a general purpose I/O (GPIO) bit.

8. The circuit of claim 2, wherein the at least one monitored signal is voltage signals and wherein the mating detection circuit comprises:

at least one FET each having its source coupled to a ground potential, its gate driven by an associated one of the at least one monitored signal, and its drain connected to a voltage source and an output node from which one of the at least one mating status signal is generated.

9. The circuit of claim 8, wherein the at least one FET comprises a plurality of FETs series connected to each other and wherein the at least one mating status signal comprises one mating status signal generated at the drain of one of the plurality of series-connected FETs located furthest from the ground potential.

10. The circuit of claim 1, wherein the mating detection circuit is located on the expansion card.

11. An expansion card for insertion into an expansion slot of a computer system, comprising:

at least one connector configured to mate with a corresponding connector of the computer system; and

a mating detector constructed and arranged to determine the mating status of a selected one or more of the at least one connector.

12. The expansion card of claim 11, wherein the mating detector is further constructed and arranged to monitor at least one signal related to an associated signal presented at each of the at least one connector.

13. The expansion card of claim 12, wherein each monitored signal is one of either the same as, provided by, derived from or controlled by the associated signal presented at each of the at least one connector.

14. The expansion card of claim 11, wherein the mating detector generates at least one mating status signal each representing the mating status of a combination of one or more of the at least one connector.

15. The expansion card of claim 14, wherein the at least one mating status signal is provided to the computer system.

16. The expansion card of claim 15, wherein the at least one mating status signal controls a state of one or more bits in the computer system.

17. The expansion card of claim 16, wherein the at least one mating status signal controls a state of a general purpose I/O (GPIO) bit.

18. The expansion card of claim 12, wherein the at least one monitored signal is voltage signals and wherein the mating detector comprises:

at least one FET each having its source coupled to a ground potential, its gate driven by an associated one of the at least one monitored signal, and its drain connected to a voltage source and an output node from which one of the at least one mating status signal is generated.

19. The expansion card of claim 18, wherein the at least one FET comprises a plurality of FETs series connected to each other and wherein the at least one mating status signal comprises one mating status signal generated at the drain of one of the plurality of series-connected FETs located furthest from the ground potential.

20. The expansion card of claim 11, wherein the at least one connector comprising one or more of the group consisting of:

at least one card connector and

at least one cable connector.

21. The expansion card of claim 20, wherein the at least one card connector comprises:

an Accelerated Graphics Port (AGP) card connector.

22. The expansion card of claim 20, wherein the at least one cable connector comprises one or more of the group consisting of:

a Universal Serial Bus (USB) cable connector; and

a power connector.

23. An expansion card for inserting into an expansion slot of a computer system, comprising:

at least one connector configured to mate with a corresponding connector of the computer system; and

means for determining whether a selected one or more of the at least one connector of the expansion card is mated with a corresponding connector of the computer system.

24. The expansion card of claim 23, wherein the determining means comprises:

means for monitoring at least one signal each related to the mating status of the selected one or more connectors; and

means for generating at least one mating status signal each representing the mating status of any combination of one or more of the selected one or more connectors.

25. The expansion card of claim 24, wherein each monitored signal is one of either the same as, provided by, derived from or controlled by the associated signal presented at each of the at least one connector.

26. The expansion card of claim 24, wherein the at least one mating status signal controls a state of one or more bits in the computer system.

27. A method for determining whether a connector of an expansion card is mated with a corresponding connector of a computer system having an expansion slot configured to receive the expansion card, comprising:

monitoring at least one signal each related to the mating status of the selected one or more connectors; and

generating at least one mating status signal each representing the mating status of any combination of one or more of the selected one or more connectors.

28. The method of claim 27, wherein each monitored signal is one of either the same as, provided by, derived from or controlled by the associated signal presented at each of the at least one connector.